Claims

1. A uniform silicon carbide single crystal with either an n-type or a p-type conductivity, **characterized by** that the crystal has a net carrier concentration less than 10^{15} cm^{-3} and a carrier lifetime of at least 50 ns at room temperature.

2. The silicon carbide crystal according to claim 1, wherein dopants conferring said n-type or p-type conductivity to the crystal are either shallow donors, comprising nitrogen, or shallow acceptors, comprising aluminum.

3. The silicon carbide crystal according to any one of claims 1 and 2, wherein the crystal is provided in the form of a wafer being sliced from an originally produced crystal.

4. The silicon carbide crystal according to claim 3, wherein the crystal is provided as a polished wafer.

5. The silicon carbide crystal according to claim 3, wherein the surface of the crystal is either off-oriented towards a Miller index direction with an off-axis angle less than 1 degree or on-axis, that is parallel to a Miller index plane.

6. The silicon carbide crystal according to any one of claims 3 to 5, wherein said wafers have a thickness that exceeds 100 µm and preferably exceeds 150 µm.

7. A method for manufacturing a silicon carbide single crystal according to claim 1, comprising the steps of:
- growing a silicon carbide single crystal, wherein:
  said crystal has a boron concentration less than $5x10^{14}$ cm^{-3} and preferably less than $5x10^{13}$ cm^{-3}, and a concentration of transition metals impurities less than $5x10^{14}$ cm^{-3} and preferably less than 10^{13} cm^{-3} ,
  the intrinsic defects in the crystal are minimised and
  said intrinsic defects comprising silicon vacancies or carbon vacancies and
- annealing, for a desired time, said crystal at a temperature above 700 °C in an atmosphere containing any of the gases:
  hydrogen,
  a mixture of hydrogen and an inert gas
so that the density of intrinsic defects and any associated defects is decreased to a concentration low enough to confer to the crystal a desired carrier life time of at least 50 ns at room temperature.

8. The method according to claim 7, further comprising the step of:
slicing and polishing a wafer from said crystal before the step of annealing the crystal.

9. The method according to claim 7, further comprising the step of:
- slicing a wafer from said crystal.

10. The method according to claim 9, further comprising the step of :
- polishing said wafer.

11. The method for growing said single crystal of silicon carbide according to claim 7, wherein the method further comprises the steps of:
- Introducing a flow of silicon and carbon atoms containing gases into an enclosure,
- Heating the enclosure containing a seed silicon carbide crystal to a temperature above 1900 °C, in such a way that the temperature of the seed crystal remains lower than the temperature at which it would decompose under the partial pressures of the Si and C containing species introduced into the heated enclosure,
- Maintaining the flows of silicon gas and carbon gas and the temperature above 1900 °C for a sufficient time so that a bulk crystal is grown and
- Introducing into the crystal, during the time of its growth, a flow of a dopant to make the crystal either n- or p-type.

12. The method according to claim 11, wherein the crystal is cooled down from the growth temperature to room temperature at a rate sufficiently slow to decrease the concentration of intrinsic levels below the concentration of shallow impurities acting as dopants.

13. The method according to claim 11, wherein the carbon containing gas is a hydrocarbon chosen from the group of methane, ethylene and propane.

14. The method according to claim 11, wherein the silicon containing gas is chosen from the group of silane, a chlorosilane compound and a methylsilane compound

15. A semiconductor device comprising:

a drift zone of a first conductivity type serving as a substrate layer having a front side and a back side,

a first contact electrode arranged at the front side of the drift zone

a control region arranged at the front side and controlling an injection of carriers of at least the first conductivity type into the drift zone

a second contact electrode at the backside of the drift zone

whereas the drift zone is arranged to carry a carrier flow between the first and the second contact electrode

characterized in that,

the drift zone consists of a silicon carbide wafer with a net carrier concentration less than 10^{15} cm^{-3} and a carrier lifetime of at least 50 ns.

16. The device according to claim 15, wherein the control region is comprising:

at least two base regions of a second conductivity type with a predetermined depth, being arranged at the front side surface within the drift zone and being separated by a space;

a source region of the first conductivity type located at the front side surface and within the base regions of the second conductivity type ;

a channel region arranged at the front side surface within the base region comprising the source region and arranged between the source region and an edge of the base region;

a gate electrode for controlling the channel region; and

a gate insulation region for electrically separating the gate electrode from the channel region.

17. A device according to claim 16, wherein the gate insulation region is located above the channel region with an overlap over the source region and completely overlapping the space between the base regions.

18. A device according to claim 16, wherein the first electrode is an emitter electrode with an ohmic contact common to the source region and the base region and being electrically isolated from the gate electrode.

19. A device according to claim 15, wherein the first electrode is an emitter electrode extending over the whole front side of the drift zone

20. A device according to claim 15, wherein the second contact electrode is a collector electrode forming a layer arranged on the surface of the backside of the drift zone.

21. A device according to claim 15, wherein a collector region is located at the backside surface within the drift zone.

22. A device according to claim 21, wherein the collector region is forming an ohmic contact with the second electrode.

23. A device according to claim 21, wherein the collector region is of a second conductivity type.

24. A device according to claim 21, wherein the collector region is extending over the whole backside of the drift zone and being provided with a field stop region.

25. A device according to claim 21, wherein the collector region is divided into several units spaced by small areas. The second contact electrode is forming an ohmic contact common with each collector unit and the drift zone or the field stop region within the drift zone.

26. A device according to claim 15, wherein the backside of the drift zone is provided with a junction termination extension for reverse blocking.

27. A device according to claim 15, wherein the front side of the drift zone is provided with a junction termination extension for forward blocking.

28. A device according to claim 15, wherein the front side of the drift zone is provided with alignment marks in order to align the structures provided on the backside of the drift zone with the structure on the front side

29. A device according to claim 15, wherein the device is an IGBT.

30. A device according to claim 15, wherein the silicon carbide wafer has a surface forming the front side or the back side surface of the drift zone and being off-oriented towards a Miller index direction with an off-axis angle less than 1 degree.

31. A device according to claim 30, wherein the surface of the silicon carbide wafer has an on-axis orientation.